National Semiconductor

March 1989

μA592 Differential Video Amplifier

General Description

The μA592 is a monolithic two-stage differential input, differential output video amplifier constructed using the Planar Epitaxial process. Internal series shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current source biased to obtain high power supply and common mode rejection ratios.

The μA592, in the 14-lead version, offers fixed gains of 100 and 400 without external components. A fixed gain of 400 is available in the 8-lead part. Adjustable gains from 0 to 400 are obtained with one external resistor.

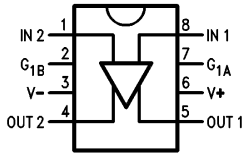
No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding. Other applications include general purpose video and pulse amplifiers.

Features

- 90 MHz bandwidth typ
- Selectable gains from 0 to 400 typ
- No frequency compensation required
- Adjustable pass band

Connection Diagrams

8-Lead DIP and SO-8 Package



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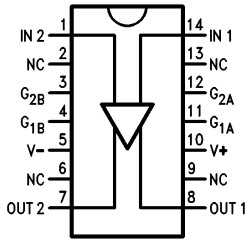
Top View

Order Number μA592SC or μA592TC
See NS Package Number M08E or N08E

14-Lead DIP



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Top View

Order Number μA592DC or μA592DM
See NS Package Number J14A

Order Information

Device Code	Package Code	Package Description
μA592TC	N08E	Molded DIP
μA592SC	M08A	Molded Surface Mount
μA592DM	J14A	Ceramic DIP
μA592DC	J14A	Ceramic DIP

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP, SO-8	−65°C to +150°C
Operating Temperature Range	
Extended (μA592M)	−55°C to +125°C
Commercial (μA592C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO Package (Soldering, 10 sec.)	265°C

Internal Power Dissipation (Notes 1, 2)	
8L-Molded DIP	0.93W
SO-8	0.81W
14L-Molded DIP	1.04W
14L-Ceramic DIP	1.36W
Supply Voltage	±8.0V
Differential Input Voltage	±5.0V
Common Mode Input Voltage	±6.0V
Output Current	10 mA

μA592 and μA592C Electrical Characteristics

$T_A = 25°C$, $V_{CC} = \pm 6.0V$ unless otherwise specified.

Symbol	Parameter	Conditions (Notes 3, 4)		μA592			μA592C			Units
				Min	Typ	Max	Min	Typ	Max	
A_{VD}	Differential Voltage Gain	$R_L = 2.0\ k\Omega$, $V_O = 3.0\ V_{P-P}$	Gain 1	300	400	500	250	400	600	V/V
			Gain 2	90	100	110	80	100	120	
B_W	Bandwidth	$R_S = 50\Omega$	Gain 1		40			40		MHz
			Gain 2		90			90		
t_r	Risetime	$R_S = 50\Omega$, $V_O = 1.0\ V_{P-P}$	Gain 1		10.5			10.5		ns
			Gain 2		4.5	10		4.5	12	
t_{PD}	Propagation Delay	$R_S = 50\Omega$, $V_O = 1.0\ V_{P-P}$	Gain 1		7.5			7.5		ns
			Gain 2		6.0	10		6.0	10	
Z_I	Input Impedance		Gain 1		4.0			4.0		kΩ
			Gain 2	20	30		10	30		
C_I	Input Capacitance		Gain 2		2.0			2.0		pF
I_{IO}	Input Offset Current				0.4	3.0		0.4	5.0	μA
I_{IB}	Input Bias Current				9.0	20		9.0	30	μA
e_n	Input Noise Voltage	$R_S = 50\Omega$, BW = 1.0 kHz to 10 MHz			12			12		μV_{rms}
V_{IR}	Input Voltage Range			±1.0			±1.0			V
CMR	Common Mode Rejection	$V_{CM} = 1.0V$, Gain 2		60	86		60	86		dB
PSRR	Power Supply Rejection Ratio	$\Delta V_{CC} = \pm 0.5V$, Gain 2		50	70		50	70		dB
V_{OO}	Output Offset Voltage		Gain 1		0.6	1.5		0.6	1.5	V
			Gain 2		0.35	0.75		0.35	0.75	
V_{OCM}	Output Common Mode Voltage			2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OP}	Output Voltage Swing			3.0	4.0		3.0	4.0		V_{P-P}
I_O-	Output Sink Current			2.5	3.6		2.5	3.6		mA
R_O	Output Resistance				20			20		Ω
I_{CC}	Supply Current				18	24		18	24	mA

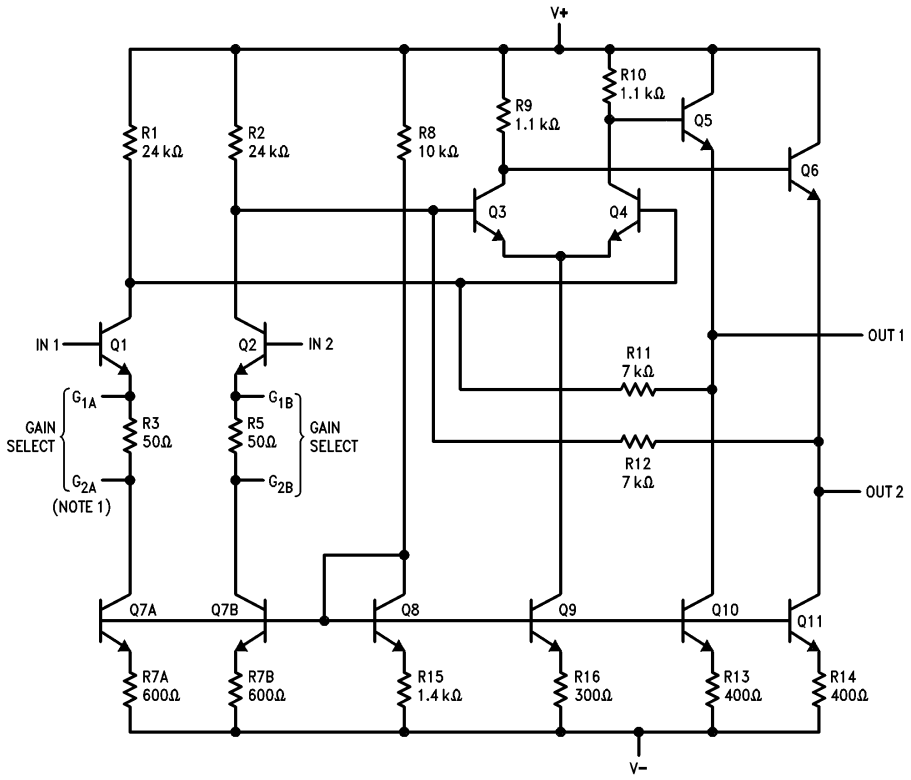
Note 1: $T_{J\ Max} = 150°C$ for the Molded DIP and SOIC, and 175°C for the Ceramic DIP.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Molded DIP at 7.5 mW/°C, the SO-8 at 6.5 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the 14L-Ceramic DIP at 9.1 mW/°C.

Note 3: Gain Select leads G_{1A} and G_{1B} connected together for Gain 1 and Gain Select leads G_{2A} and G_{2B} connected together for Gain 2.

Note 4: Gain 2 not applicable to 8 lead device.

Equivalent Circuit



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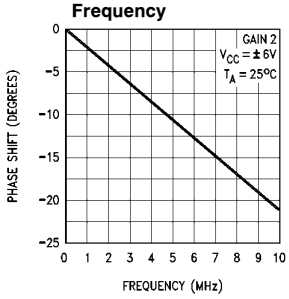
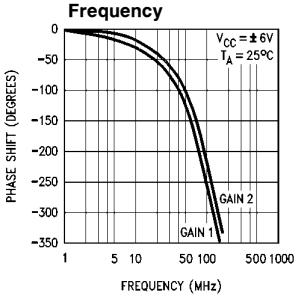
Note 1: G_{2A} and G_{2B} applies to 14 lead device only.

Typical Performance Curves

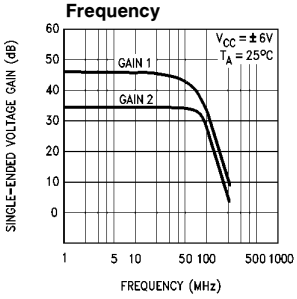
Phase Shift vs Frequency



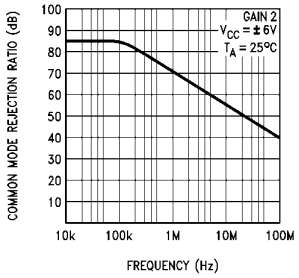
Phase Shift vs Frequency



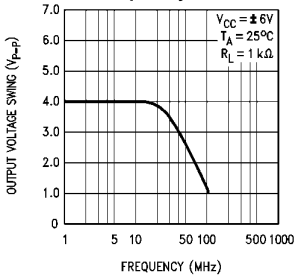
Voltage Gain vs Frequency



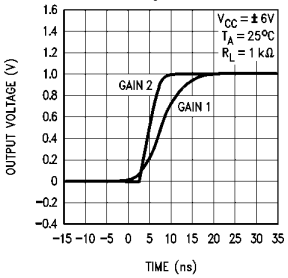
Common Mode Rejection Ratio vs Frequency



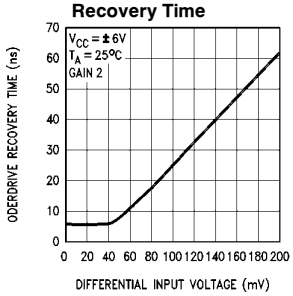
Output Voltage Swing vs Frequency



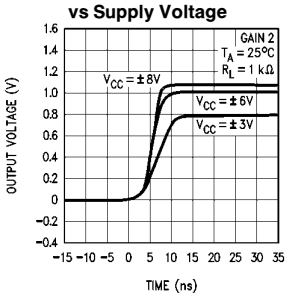
Pulse Response



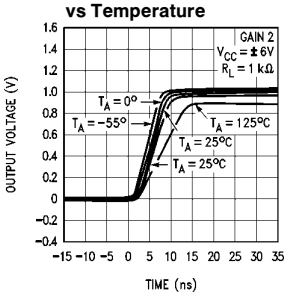
Differential Overdrive Recovery Time



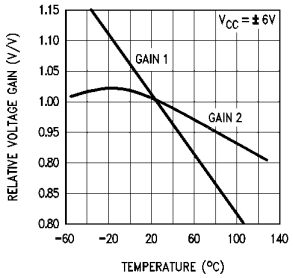
Pulse Response vs Supply Voltage



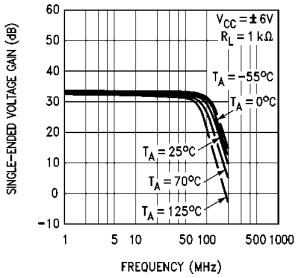
Pulse Response vs Temperature



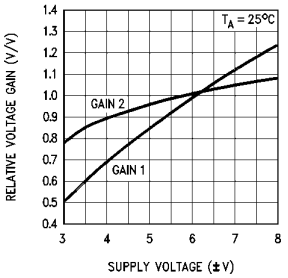
Voltage Gain vs Temperature



Gain vs Frequency vs Temperature



Voltage Gain vs Supply Voltage



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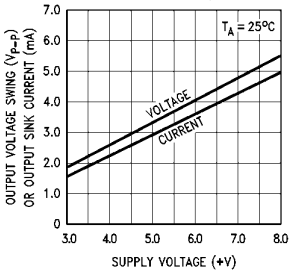
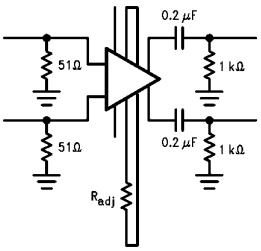
Typical Performance Curves (Continued)

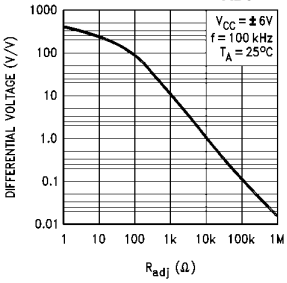
Output Voltage and Current Swing vs Supply Voltage



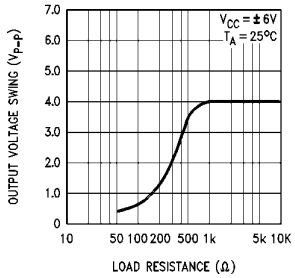
Voltage Gain Adjust Circuit



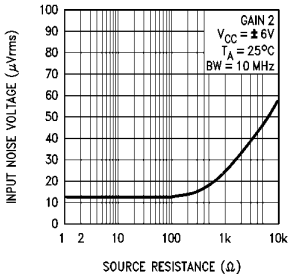
Voltage Gain vs R_{ADJ}



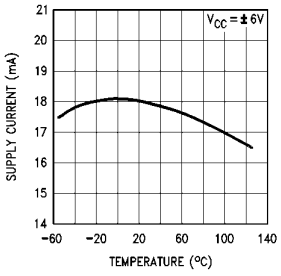
Output Voltage Swing vs Load Resistance



Input Noise Voltage vs Source Resistance



Supply Current vs Temperature



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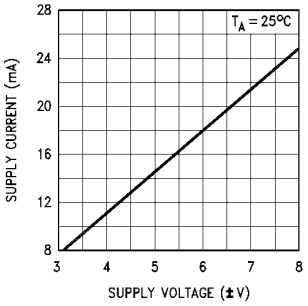
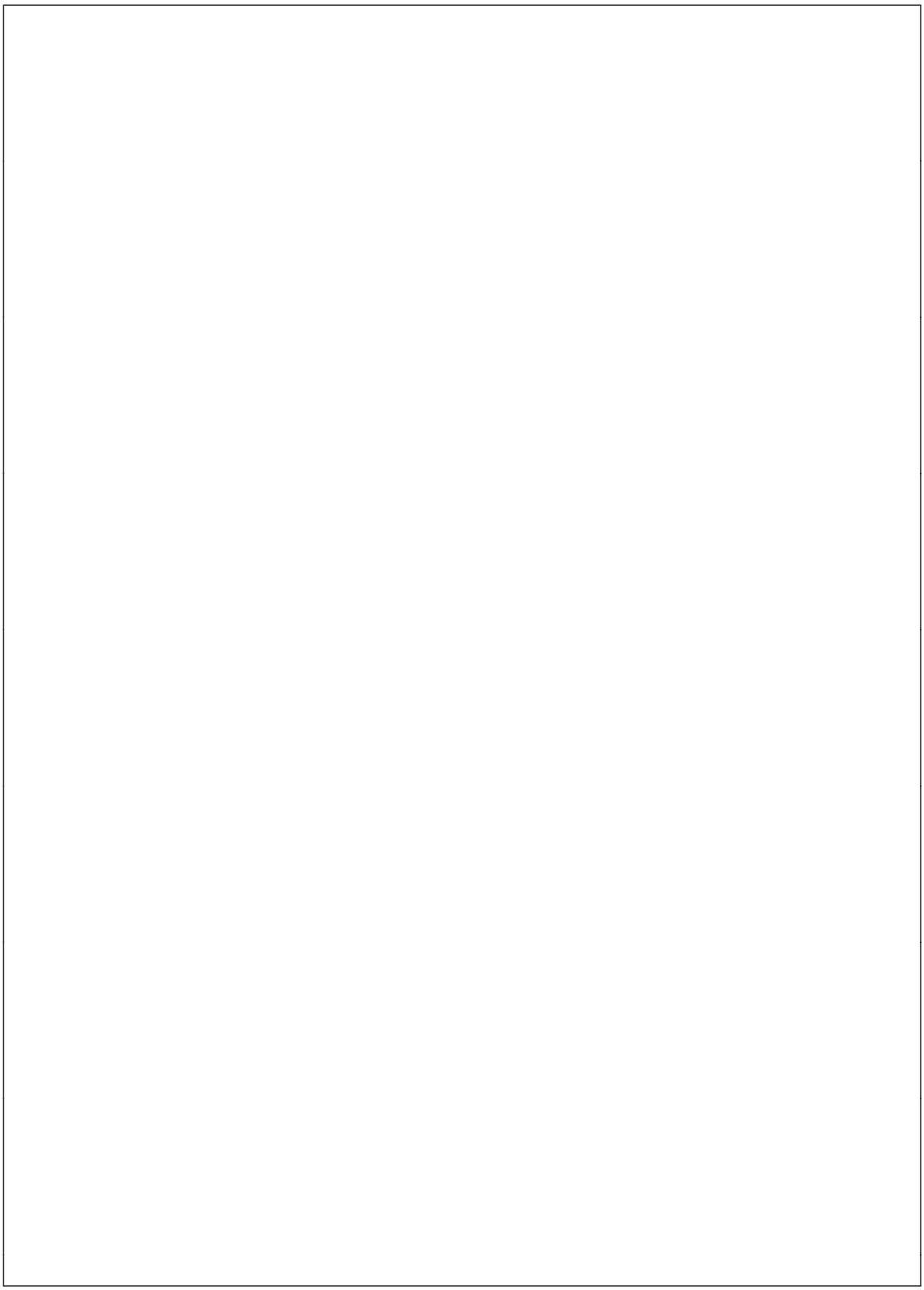
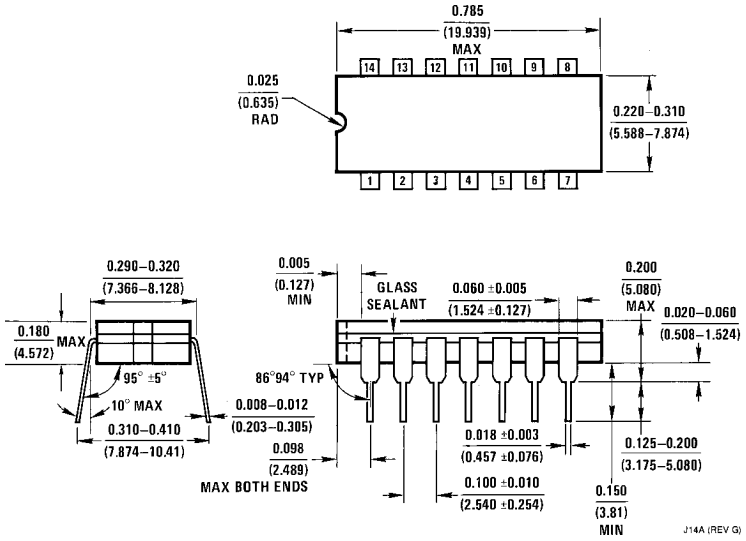
Supply Current vs Supply Voltage



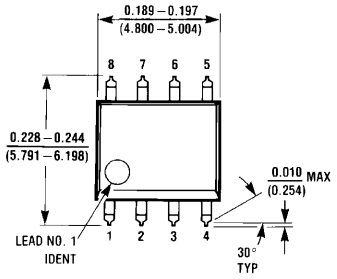
TL/H/10047–6

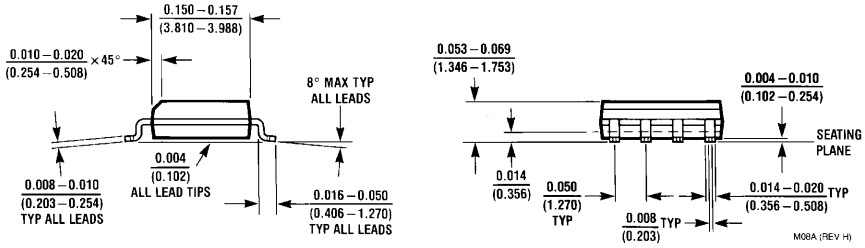


Physical Dimensions inches (millimeters)



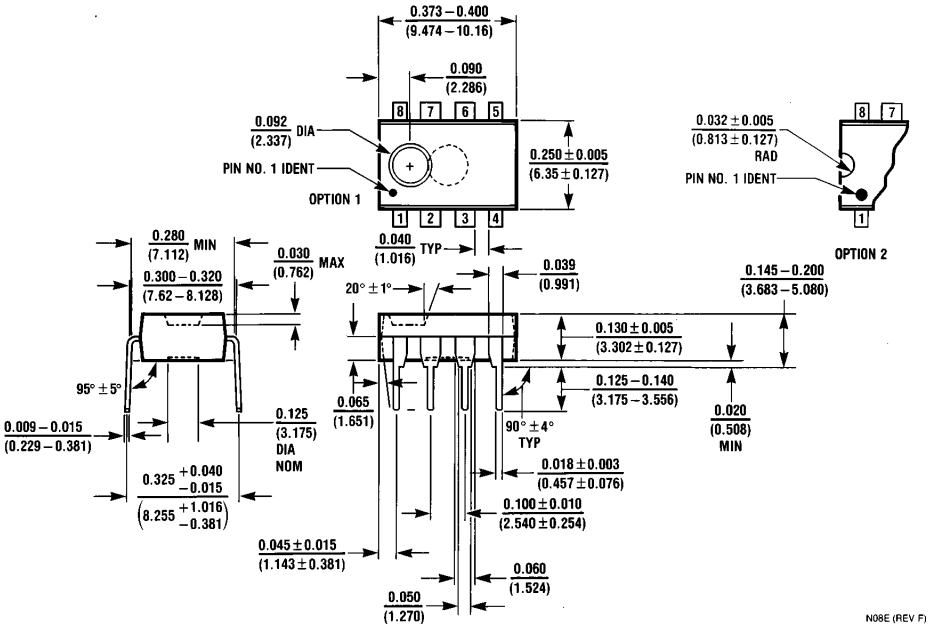
14-Lead Ceramic Dual-In-Line Package (J)
Order Number μA592DC or μA592DM
NS Package Number J14A





8-Lead Molded Surface Mount (M)
Order Number μA592SC
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



8-Lead Molded Dual-In-Line Package (N)
Order Number μA592TC
NS Package Number N08E

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