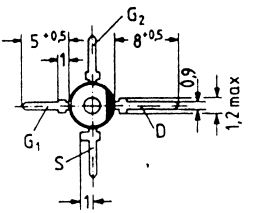
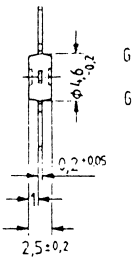
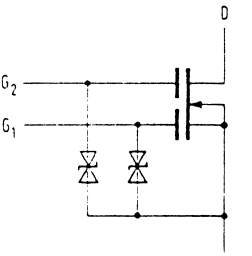
# MOS Field Effect Transistor

BF 961 is an ion-implanted dual gate N channel MOS field effect transistor of the depletion type with integrated gate protection diodes in a plastic package similar to TO 120 (50 B 4 DIN 41876). The source terminal is internally connected with the substrate. The tetrode is especially suitable for use in TV VHF input stages and mixers.

| Type | Ordering code |
|---|---|
| BF 961 | Q62702-F518 |




Approx. weight 0.35 g
Dimensions in mm

Circuit diagramm:

## Maximum ratings

| | | | |
|---|---|---|---|
| Drain source voltage | $V_{DS}$ | 20 | V |
| Drain current | $I_D$ | 30 | mA |
| Gate 1/gate 2 source peak current | $\pm I_{G1/2SM}$ | 10 | mA |
| Storage temperature range | $T_{stg}$ | −55 to +150 | °C |
| Channel temperature | $T_{ch}$ | 150 | °C |
| Power dissipation | $P_{tot}$ | 200 | mW |

## Thermal resistance

| | | | |
|---|---|---|---|
| Channel to ambient | $R_{thA}$ | ≦ 450 | K/W |

## Static characteristics ($T_{amb}$ = 25 °C)

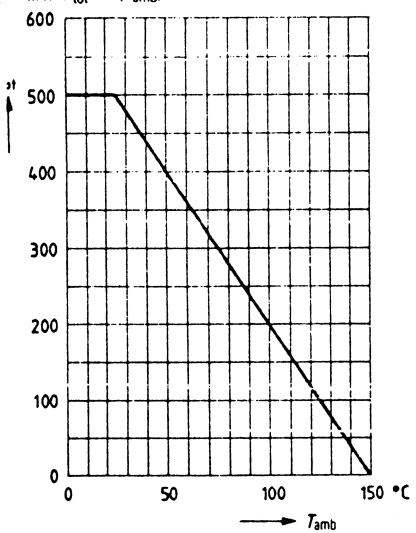
| | | | |
|---|---|---|---|
| Drain-source breakdown voltage ($I_D$ = 10 µA; $-V_{G1S}$ = $-V_{G2S}$ = 4 V) | $V_{(BR)DS}$ | ≧ 20 | V |
| Gate 1 source breakdown voltage ($\pm I_{G1S}$ = 10 mA; $V_{G2S}$ = $V_{DS}$ = 0) | $\pm V_{(BR)G1SS}$ | 6 to 20 | V |
| Gate 2 source breakdown voltage ($\pm I_{G2S}$ = 10 mA; $V_{G1S}$ = $V_{DS}$ = 0) | $\pm V_{(BR)G2SS}$ | 6 to 20 | V |
| Gate 1 leakage current ($\pm V_{G1S}$ = 5 V; $V_{G2S}$ = $V_{DS}$ = 0) | $I_{G1SS}$ | ≦ 50 | nA |
| Gate 2 leakage current ($\pm V_{G2S}$ = 5 V; $V_{G1S}$ = $V_{DS}$ = 0) | $I_{G2SS}$ | ≦ 50 | nA |
| Drain current ($V_{DS}$ = 15 V; $V_{G1S}$ = 0; $V_{G2S}$ = 4 V) | $I_{DSS}$ | 4 to 20 | mA |
| Gate 1 source pinch-off voltage ($V_{DS}$ = 15 V; $V_{G2S}$ = 4 V; $I_D$ = 20 µA) | $-V_{G1S(p)}$ | 0.2 to 3.5 | V |
| Gate 2 source pinch-off voltage ($V_{DS}$ = 15 V; $V_{G1S}$ = 0; $I_D$ = 20 µA) | $-V_{G2S(p)}$ | 0.2 to 3.5 | V |

**Dynamic characteristics** ($T_{amb}$ = 25 °C)

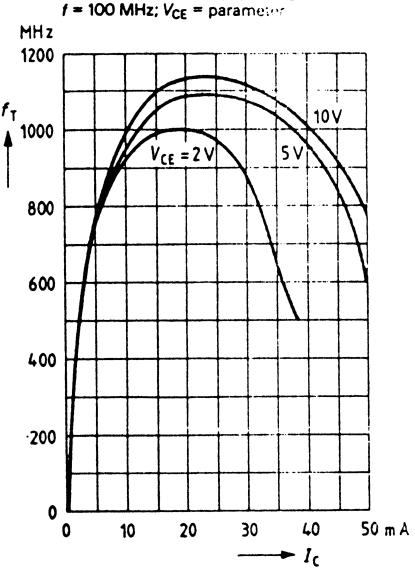
| | | | |
|---|---|---|---|
| **Forward transadmittance** ($V_{DS}$ = 15 V; $I_D$ = 10 mA; $V_{G2S}$ = 4 V; $f$ = 1 kHz) | $g_{fs}$ | 15 (12 to 20) | mS |
| **Gate 1 input capacitance** ($V_{DS}$ = 15 V; $I_D$ = 10 mA; $V_{G2S}$ = 4 V; $f$ = 1 MHz) | $C_{G1sS}$ | 3.6 (3 to 4.5) | pF |
| **Gate 2 input capacitance** ($V_{DS}$ = 15 V; $I_D$ = 10 mA; $V_{G2S}$ = 4 V; $f$ = 1 MHz) | $C_{G2sS}$ | 1.6 | pF |
| **Reverse transfer capacitance** *) ($V_{DS}$ = 15 V; $I_D$ = 10 mA; $V_{G2S}$ = 4 V; $f$ = 1 MHz) | $C_{dg1}$ | 25 (≤ 35) | fF |
| **Output capacitance** ($V_{DS}$ = 15 V; $I_D$ = 10 mA; $V_{G2S}$ = 4 V; $f$ = 1 MHz) | $C_{dsS}$ | 1.6 (1.2 to 2.2) | pF |
| **Power gain** ($V_{DS}$ = 15 V; $I_D$ = 10 mA; $f$ = 200 MHz; 2 $\Delta f$ = 12 MHz) | $G_{ps}$ | 23 (≥ 19) | dB |
| **Noise figure** ($V_{DS}$ = 15 V; $I_D$ = 10 mA; $f$ = 200 MHz; $g_G$ = 2 mS; test circuit[1]) | $NF$ | 1.8 (≤ 2.8) | dB |
| **Control range** ($V_{DS}$ = 15 V; $V_{G2}$ = 4 to −2 V; $f$ = 200 MHz; Test circuit 1) | $\Delta G_{ps}$ | 50 | dB |
| **Mixer gain (additive)** ($V_D$ = 15 V; $V_{G2}$ = 6 V, $R_S$ = 220 Ω; $f$ = 200 MHz; $f_{IF}$ = 36 MHz; 2 $\Delta f_{IF}$ = 5 MHz; $V_{OSC}$ = 0.5 V; Test circuit 2) | $G_{psC}$ | 16 | dB |
| **Mixer gain (multiplicative)** ($V_D$ = 15 V; $V_{G1}$ = 1.7 V, $V_{G2}$ = 2.5 V $R_S$ = 220 Ω; $f$ = 200 MHz; $f_{IF}$ = 36 MHz 2 $\Delta f_{IF}$ = 5 MHz; $V_{OSC}$ = 2 V Test circuit 3) | $G_{FSC}$ | 18 | dB |

*) $G_2$ S on screen potential

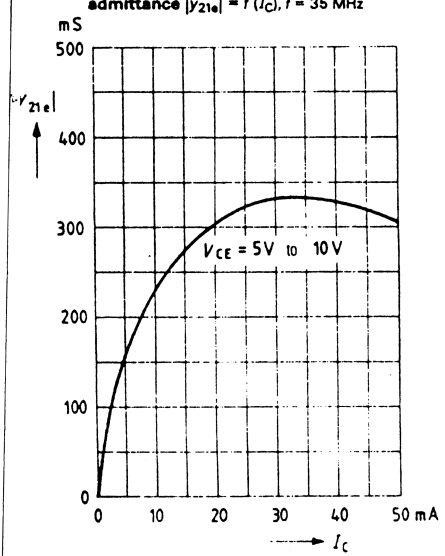
**Total perm. power dissipation versus temperature**
$P_{tot} = f(T_{amb})$



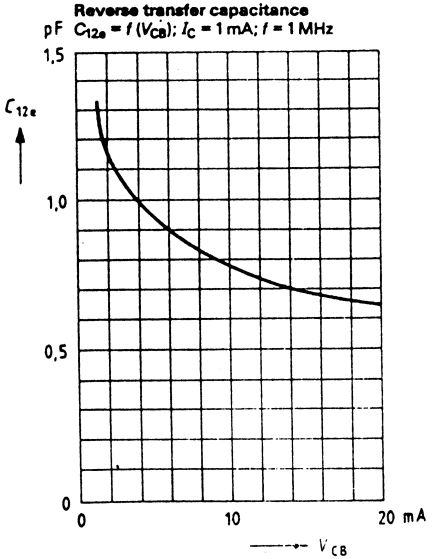

**Transition frequency $f_T = f(I_C)$**
$f$ = 100 MHz; $V_{CE}$ = parameter




**Short-circuit forward transfer admittance $|y_{21e}| = f(I_C)$, $f$ = 35 MHz**

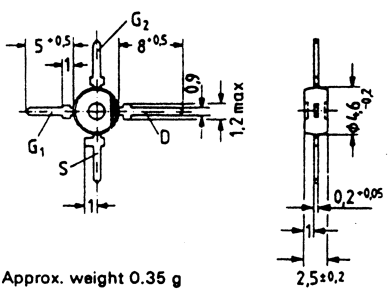



**Reverse transfer capacitance**
$C_{12e} = f(V_{CB})$; $I_C$ = 1 mA; $f$ = 1 MHz



BF 960 is an ion-implanted dual gate N-channel MOS field effect transistor of the depletion type with integrated gate-protection diodes in a plastic package similar to TO 120, (50 B4 DIN 41 867). The source lead is internally connected with the substrate.
The BF 960 tetrode is particularly suitable for use in TV UHF input stages and mixers as well as for universal applications throughout the frequency range between 200 MHz and 1 GHz.

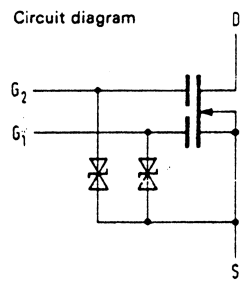
| Type | Ordering code |
|---|---|
| BF 960 | Q62702-F499 |




Approx. weight 0.35 g

Dimensions in mm

Circuit diagram




**Maximum ratings**

| | | | |
|---|---|---|---|
| Drain-source voltage | $V_{DS}$ | 20 | V |
| Drain current | $I_D$ | 30 | mA |
| Gate 1/gate 2-source peak current | $\pm I_{G1/2SM}$ | 10 | mA |
| Storage temperature range | $T_{stg}$ | −55 to +150 | °C |
| Channel temperature | $T_{ch}$ | 150 | °C |
| Total power dissipation ($T_{amb} \leq 60$°C) | $P_{tot}$ | 200 | mW |

**Thermal resistance**

| | | | |
|---|---|---|---|
| Channel to ambient | $R_{thA}$ | ≤450 | K/W |

**Static characteristics** ($T_{amb}$ = 25 °C)

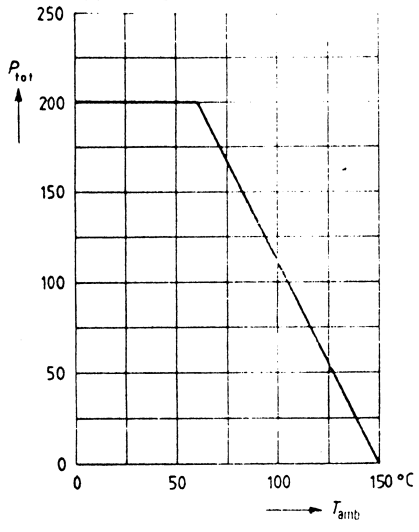
| | | | |
|---|---|---|---|
| Drain-source breakdown voltage ($I_D$ = 10 μA; $-V_{G1S}$ = $-V_{G2S}$ = 4 V) | $V_{(BR)DS}$ | ≥ 20 | V |
| Gate 1 source breakdown voltage ($\pm I_{G1S}$ = 10 mA; $V_{G2S}$ = $V_{DS}$ = 0) | $\pm V_{(BR)G1SS}$ | 6 to 20 | V |
| Gate 2 source breakdown voltage ($\pm I_{G2S}$ = 10 mA; $V_{G1S}$ = $V_{DS}$ = 0) | $\pm V_{(BR)G2SS}$ | 6 to 20 | V |
| Gate 1 leakage current ($\pm V_{G1S}$ = 5 V; $V_{G2S}$ = $V_{DS}$ = 0) | $\pm I_{G1SS}$ | < 50 | nA |
| Gate 2 leakage current ($\pm V_{G2S}$ = 5 V; $V_{G1S}$ = $V_{DS}$ = 0) | $\pm I_{G2SS}$ | < 50 | nA |
| Drain current ($V_{DS}$ = 15 V; $V_{G1S}$ = 0; $V_{G2S}$ = 4 V) | $I_{DSS}$ | 2 to 20 | mA |
| Gate 1 source pinch-off voltage ($V_{DS}$ = 15 V; $V_{G2S}$ = 4 V; $I_D$ = 20 μA) | $-V_{G1S(p)}$ | ≤ 2.7 | V |
| Gate 2 source pinch-off voltage ($V_{DS}$ = 15 V; $V_{G1S}$ = 0; $I_D$ = 20 μA) | $-V_{G2S(p)}$ | ≤ 2.7 | V |

**Dynamic characteristics** ($T_{amb}$ = 25 °C)

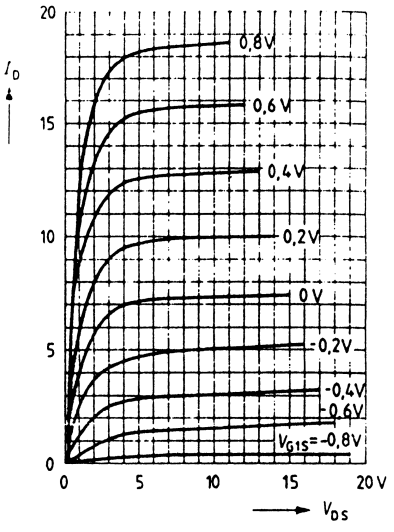
| | | | |
|---|---|---|---|
| Forward transadmittance<br>($V_{DS}$ = 15 V; $I_D$ = 7 mA; $V_{G2S}$ = 4 V; $f$ = 1 kH) | $g_{fs}$ | 12 (9.5 to 18) | mS |
| Gate 1 input capacitance<br>($V_{DS}$ = 15 V; $I_D$ = 7 mA; $V_{G2S}$ = 4 V; $f$ = 1 MHz) | $C_{g1ss}$ | 1.8 (1.3 to 2.3) | pF |
| Gate 2 input capacitance<br>($V_{DS}$ = 15 V; $I_D$ = 7 mA; $V_{G2S}$ = 4 V; $f$ = 1 MHz) | $C_{g2ss}$ | 1 | pF |
| Reverse transfer capacitance *)<br>($V_{DS}$ = 15 V; $I_D$ = 7 mA; $V_{G2S}$ = 4 V; $f$ = 1 MHz) | $C_{dg1}$ | 25 (<35) | fF |
| Output capacitance<br>($V_{DS}$ = 15 V; $I_D$ = 7 mA; $V_{G2S}$ = 4 V; $f$ = 1 MHz) | $C_{dss}$ | 0.8 (0.65 to 1.2) | pF |
| Power gain<br>($V_{DS}$ = 15 V; $I_D$ = 7 mA) | | | |
| at $f$ = 200 MHz; $G_G$ = 2 mS; $G_L$ = 0.5 mS | $G_{ps}$ | 23 | dB |
| at $f$ = 800 MHz; $G_G$ = 2 mS; $G_L$ = 1 mS | $G_{ps}$ | 16.5 (13 to 20) | dB |
| Noise figure<br>($V_{DS}$ = 15 V; $I_D$ = 7 mA; $g_G$ = 2 mS) | | | |
| at $f$ = 200 MHz | $NF$ | 1.6 (<2.8) | dB |
| at $f$ = 800 MHz | $NF$ | 2.8 (<3.9) | dB |
| Control range<br>($V_{DS}$ = 15 V; $V_{G2}$ = 4 to −2 V; $f$ = 800 MHz) | $\Delta G_{ps}$ | >40 | dB |
| Mixer gain<br>($V_{DS}$ = 15 V; $V_{G2}$ = 4 V; $f$ = 800 MHz;<br>$f_{IF}$ = 36 MHz; $2\Delta f_{IF}$ = 5 MHz;<br>$V_{osc.}$ = 800 mV) | $G_{psc}$ | 16 | dB |

*) $G_1$ and S on screen potential

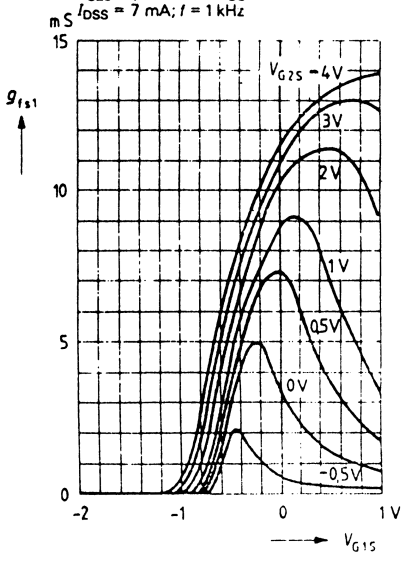
**Total perm. power dissipation versus temperature**
$P_{tot} = f(T_{amb})$



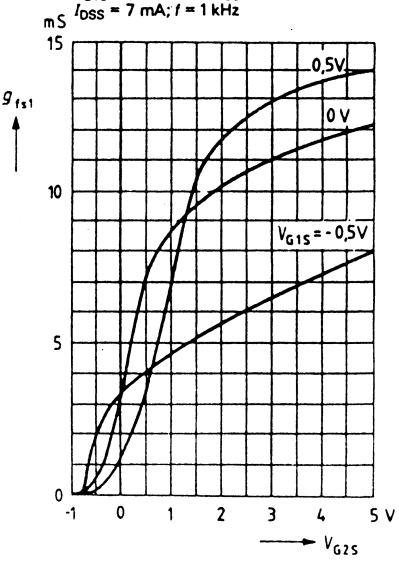

**Family of output characteristics**
$I_D = f(V_{DS})$; $V_{G1S}$ = parameter;
$V_{G2S}$ = 4 V



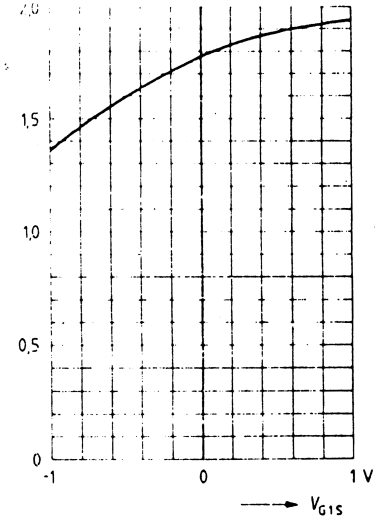

**Gate 1 transadmittance** $g_{fs1} = f(V_{G1S})$;
$V_{G2S}$ = parameter; $V_{DS}$ = 15 V
$I_{DSS}$ = 7 mA; $f$ = 1 kHz



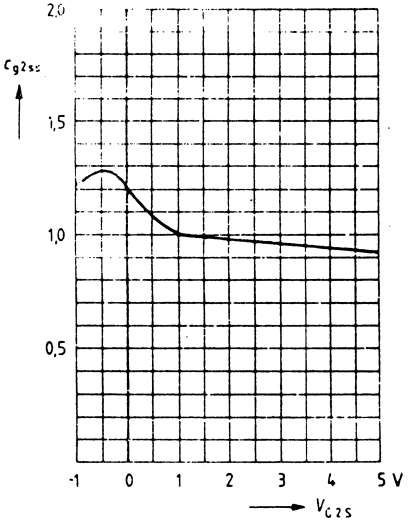

**Gate 2 transadmittance** $g_{fs1} = f(V_{G2S})$
$V_{G1S}$ = parameter; $V_{DS}$ = 15 V;
$I_{DSS}$ = 7 mA; $f$ = 1 kHz



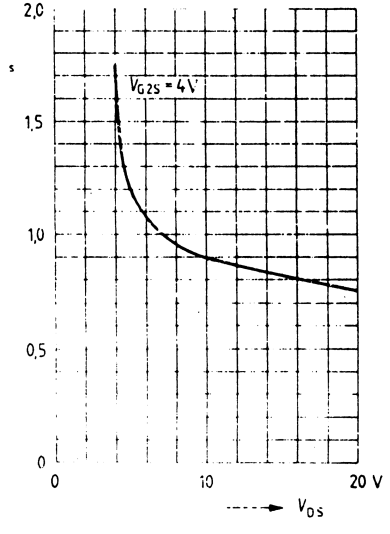
**Gate 1 input capacitance**
$C_{g1ss} = f(V_{G1})$, $V_{G2S} = 4$ V;
$V_{DS} = 15$ V; $f = 1$ MHz



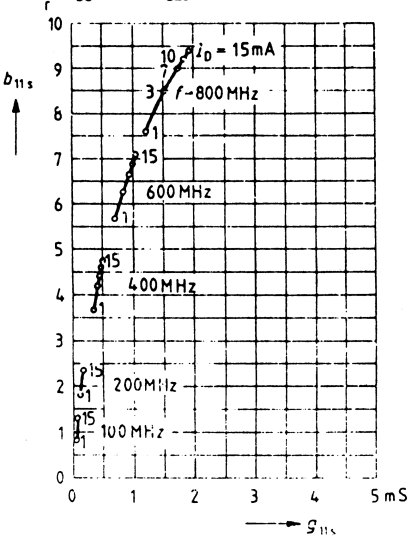

**Gate 2 input capacitance**
$C_{g2ss} = f(V_{G2S})$; $V_{G1S} = 0$
$V_{DS} = 15$ V; $f = 1$ MHz



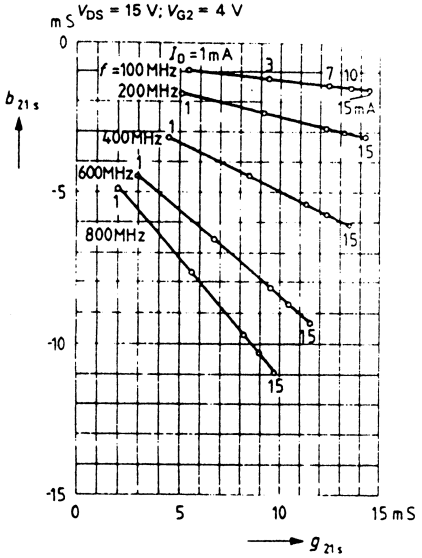

**Output capacitance**
$C_{dss} = f(V_{DS})$; $V_{G1S} = 0$
$V_{G2S} = 4$ V; $f = 1$ MHz



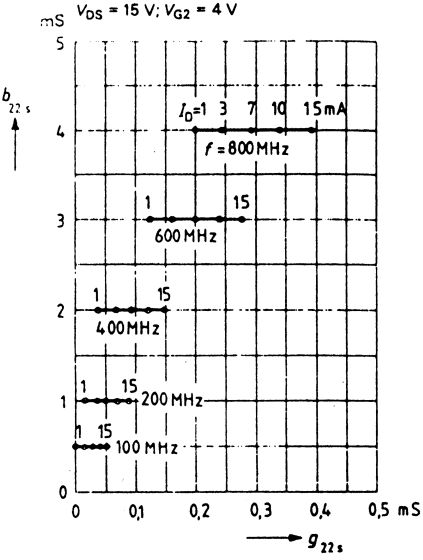

**Gate 1 input conductance $y_{11s}$**
(source circuit)
$V_{DS} = 15$ V; $V_{G2S} = 4$ V



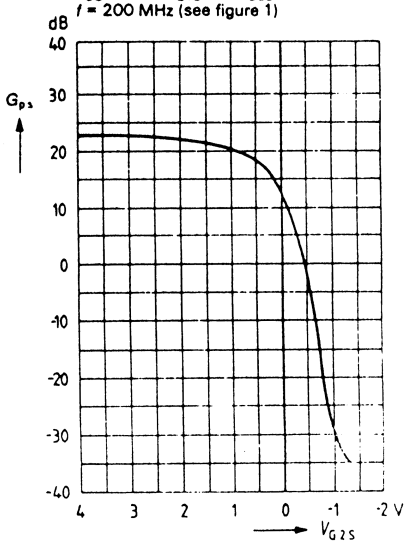
**Gate 1 transadmittance $Y_{21s}$**
(source circuit)
$V_{DS}$ = 15 V; $V_{G2}$ = 4 V



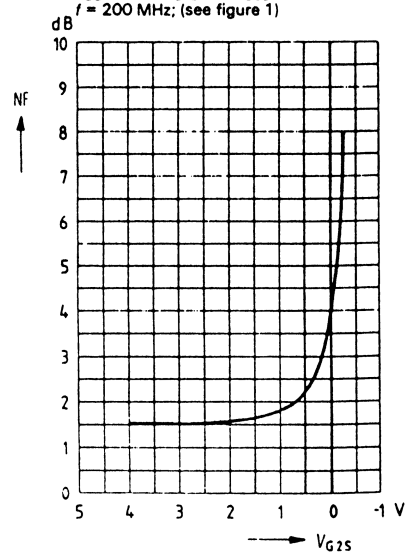

**Output conductance $Y_{22s}$**
(source circuit)
$V_{DS}$ = 15 V; $V_{G2}$ = 4 V



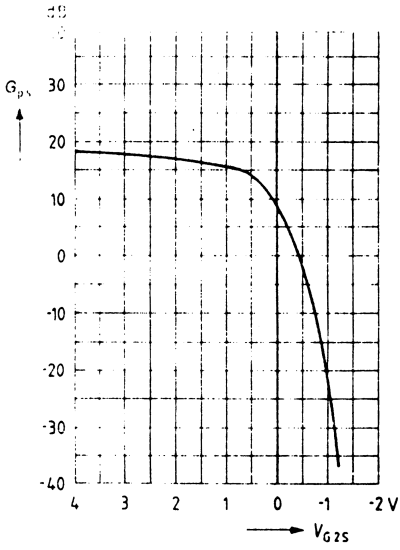

**Power gain $G_{ps}$ = f ($V_{G2S}$);**
$V_{DS}$ = 15 V; $V_{G1S}$ = 0; $I_{DSS}$ = 7 mA;
f = 200 MHz (see figure 1)



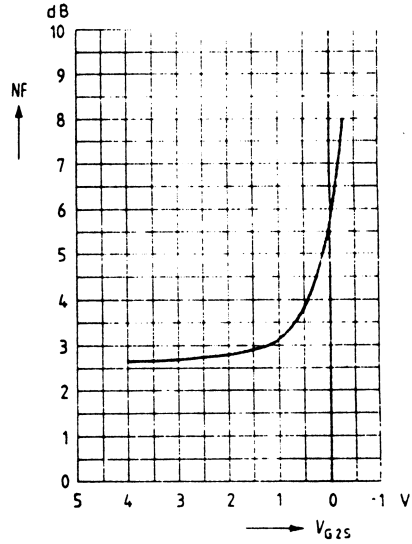

**Noise figure NF = f ($V_{G2S}$)**
$V_{DS}$ = 15 V; $V_{G1S}$ = 0; $I_{DSS}$ = 7 mA;
f = 200 MHz; (see figure 1)



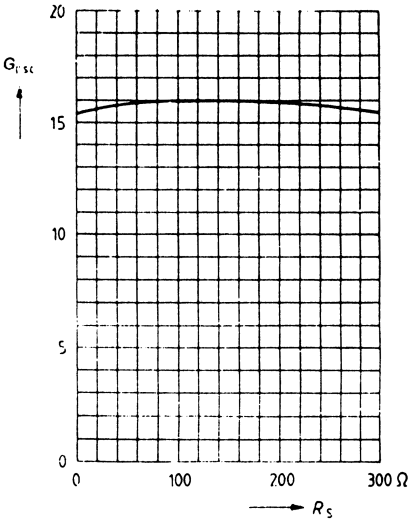
**Power gain** $G_{ps} = f(V_{G2S})$
$V_{DS}$ = 15 V; $V_{G1S}$ = 0;
$I_{DSS}$ = 7 mA; $f$ = 800 MHz; $R_S$ = 0
(see figure 2)



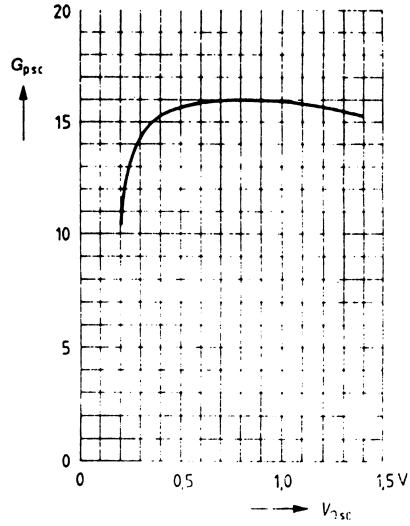

**Noise figure** $NF = f(V_{G2S})$
$V_{DS}$ = 15 V; $V_{G1S}$ = 0;
$I_{DSS}$ = 7 mA; $f$ = 800 MHz; $R_S$ = 0
(see figure 2)



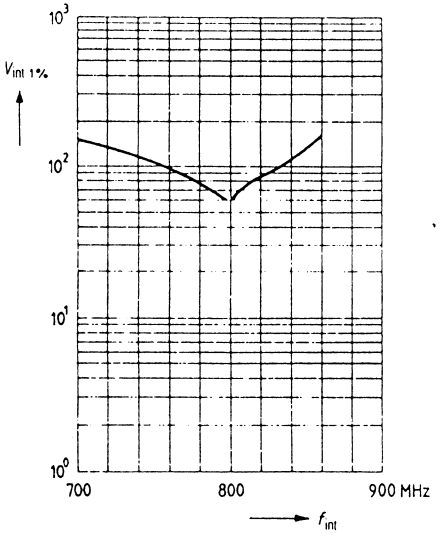

**Mixer gain** $G_{psc} = f(R_S)$
$f_e$ = 800 MHz; $f_{osc}$ = 836 MHz
$V_{osc}$ = 800 mV; $V_{DS}$ = 15 V
$V_{G2S}$ = 4 V; $I_{DSS}$ = 7 mA
dB (see figure 3)



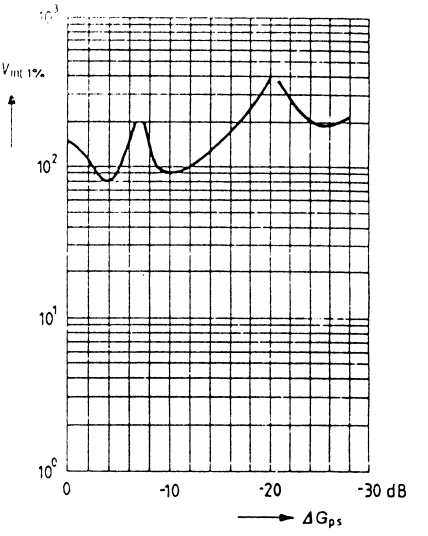

**Mixer gain** $G_{psc} = f(V_{osc})$
$f_e$ = 800 MHz; $f_{osc}$ = 836 MHz
$V_{DS}$ = 15 V; $V_{G2S}$ = 4 V;
$I_{DSS}$ = 7 mA; $R_S$ = 150 Ω
dB (see figure 3)



**Interference voltage for 1% cross modulation** $V_{int\ 1\%} = f(f_{int})$[1]; $m_{int}$ = 100%; $V_{DS}$ = 15 V; $V_{G2}$ = 4 V; $V_{G1}$ = 1 V; $R_S$ = 150 Ω (see figure 2)

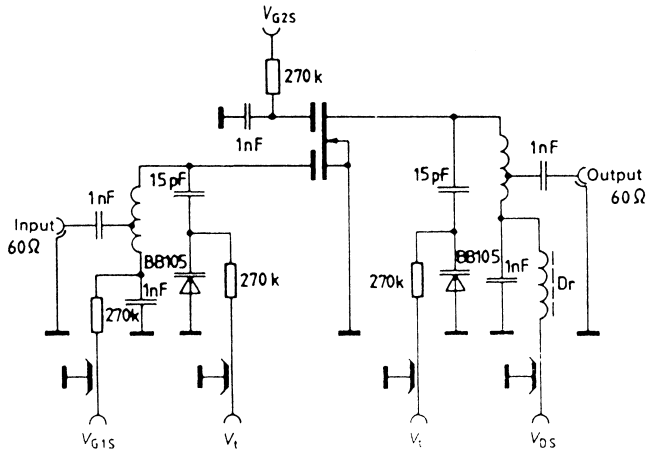



**Interference voltage for 1% cross modulation** $V_{int\ 1\%} = f(G_p)$[1]; $f_w$ = 800 MHz; $f_{int}$ = 700 MHz; $m_{int}$ = 100%; $V_{DS}$ = 15 V; $V_{G1}$ = 1 V; $R_S$ = 150 Ω (see figure 2)




**Test circuit for power gain and noise figure** at $f$ = 200 MHz ($G_G$ = 2 ms; $G_L$ = 0.5 mS)

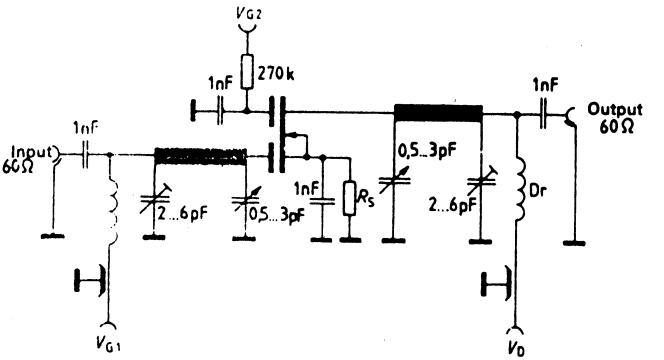
Fig. 1




1) $V_{int\ 1\%}$ is the rms value of half the EMC (terminal voltage at matching) of a 100% sine modulated TV carrier at an internal generator resistance of 60 Ω, causing 1% amplitude modulation on the active carrier.

Test circuit for power gain, **noise figure and cross modulation**
$f$ = 800 MHz; $G_g$ = 2 mS; $G_g$ = 1 mS.

Fig. 2




**Test circuit for mixer gain $f$ = 800/36 MHz.**

Fig. 3